Fourth semester B Tech degree examination,April 2015
(2013 Scheme)
Branch : Electronics & Communication Engg
13.406 Analog Integrated Circuits (T)

Time : 3 hrs **Max marks : 100**

Model Question Paper

Part A (Answer all questions)

1. Differential gain of an op amp measures 100. In the measurement of common mode gain experiment when 1.0V is applied common to both the inputs , output voltage measured is 0.01V.How much is CMRR?
2. How does input offset voltage in an op amp arise? And how can it be corrected?
3. Give the limitations of an ideal integrator.
4. What is roll- off rate of a first order filter?
5. Why is the state variable filter called universal filter?
6. What is hysteresis? What parameters determine hysteresis?
7. Why is an inverted R-2R ladder network DAC better than R-2R ladder DAC?
8. If a 10 bit D/A converter spans a range of 0 to 10 V and is always within 1mV of its ideal output, What is its linearity as a percent of full scale range?
9. Give the basic difference between digital and analog PLLs.
10. State the limitations of linear voltage regulators.

(10 x 2 =20)

Part B (Answer any one question from each module (1 x 20)

Module I

11. a)What is voltage to current converter? How can an opamp be ued as a voltage to current converter for grounded load and floating load? (10)

    b)With the help of a circuit ,explain how opamp can be used as inverting adder .Draw an opamp circuit whose output is $v_1 - v_2 + v_3 - v_4$ (10)

12. a)With the help of a circuit ,explain folded cascade CMOS opamp. (10)
    b) i)Define slew rate. How it is measured? (5)
    ii) A 741C opamp is used as an inverting amplifier with a gain of 50.The voltage gain Vs frequency curve of 741c is flat upto 20 Khz. What maximum peak to peak input signal can be applied without distorting the output? (5)

Module II

13. a) A first order low pass butterworth filter has a cut off frequency of 12 Khz and unity gain at low frequency. Find the voltage transfer function magnitude in dB at 15 Khz for the filter. (10)

b) Explain the operation of a square wave generator by drawing the capacitor and output voltage waveforms. (10)

14.a) Design a monostable multivibrator for 0.6 s ON time. (10)

b) Outline the process for creating higher order filters and explain why cascades of similar order filters donot give appropriate results. (10)

Module III

15.a) An 8 bit A/D converter accepts an input voltage signal of range 0 to 12 V.

What is the minimum value of input voltage required to generate a change of 1 LSB? (3)

What input voltage will generate all 1's at A/D converter output? (3)

What is the digital output for an input voltage of 6V? (4)

b) Explain the operation of switched capacitor integrator with neat figures. (10)

16 .a) For a 4 bit R-2R ladder D/A converter assume that the full scale voltage is 10V. Calculate the step change in output voltage when input changes from 1001 to 1110. (10)

b) Design a 3 bit simultaneous type A/D converter. (10)

Module IV

17.a)Using 7805 voltage regulator,design a current source to deliver 400mA current to a 50 ohm ,5W load. (10)

b) Find the lock and capture frequencies for PLL 565,with free running frequency of 120Khz,demodulation capacitor of 1μF and supply voltage of +/- 5V. (10)

18.a)Explain the circuit operation of a high voltage regulator using IC 723 with a circuit diagram. Write the equation for output voltage , its range and current that can be obtained using the circuit. (10)

b) Explain how a four quadrant multiplier can be obtained from single quadrant multipliers (10)