

Reg. No.:



Name:

University of Kerala

U8871

Second Semester FYUGP Degree Examination, April 2025

Discipline Specific Core Course

ELECTRONICS

UK2DSCELE102 - Fundamentals of Digital Technology

Academic Level: 100-199

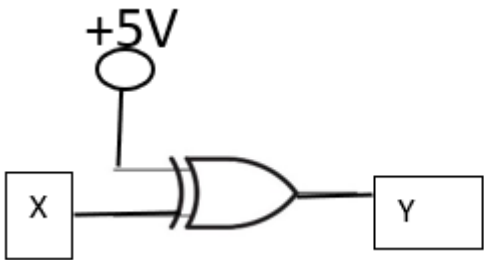
Time: 2 Hours(120 Mins)

Max. Marks: 56

Part A.6 Marks:Time 5 Minutes.(Cognitive Level :Remember(RE)/Understand(UN)) Objective Type.1 mark each, Answer all questions

Qn No.	Question	CL	CO
1	Multiplexers is also known as_____	RE	4
2	Give an example for a sequential circuit.	RE	3
3	Summarize the purpose of using a K-Map in simplifying Boolean expressions.	UN	1
4	Digital multiplexer is basically a combinational logic circuit to perform the operation Options : A) AND – AND B)OR – OR C) AND – OR D)OR - AND	UN	4
5	Describe the output behavior of a JK flip-flop when both inputs (J and K) are high.	UN	3
6	Classify the following gates in to basic and universal: AND, NAND, NOR	UN	2

Part B.10 Marks.Time:20 Minutes (Cognitive Level:Understand(UN)/Apply(AP))Two-three sentences.2 marks each.Answer all questions

Qn No.	Question	CL	CO
7	Explain De Morgan's theorem for the OR operation.	UN	1
8	Explain how OR gate is realized using NAND gate with truth table	UN	2
9	Demonstrate the operation of the comparator with a functional diagram	AP	4
10	 Predict the gate and write its truth table	AP	2
11	Convert the decimal number 25 to its binary equivalent.	AP	1

Part C.16 Marks.Time:35 Minutes.(Cognitive Level :Apply(AP)/Analyse(AN))Short Answer.4 marks each, Answer all 4 questions,choosing among options * within each question

Qn No.	Question	CL	CO
12	A)	AP	4, 5

Qn No.	Question	CL	CO
	Apply the logic of a 1-to-8 demultiplexer to route an input signal to output Y6 when select lines are set to 110. Show the logic diagram and explain the result. OR B) Demonstrate the working of Delay Flip Flop using its circuit diagram and truth table		
13	A) Convert the hexadecimal number 2F3 into its octal equivalent using an intermediate binary representation. Show all steps clearly. OR B) Design a logic circuit using basic logic gates (AND, OR, NOT) to implement the Boolean expression $Y = A.B + A'.C$. Draw the circuit diagram and create the truth table to demonstrate the circuit's behavior for all possible input combinations.	AP	1, 2
14	A) Convert the following decimal number to binary and octal number system (i) $(456)_{10}$ (ii) $(1027)_{10}$ OR B) Implement the AND gate using only NAND gates.	AN	1, 1
15	A) Examine the working a half adder circuit and represent it using AND and XOR gates. OR B) Analyse a 2-bit comparator circuit to determine which of two 2-bit binary numbers is greater, equal, or smaller.	AN	3, 4

Part D.24 Marks.Time: 60 Minutes.(Cognitive Level :Analyse(AN)/Evaluate(EV)/Create(CR)) Long Answer 6 Marks each.Answer all 4 questions choosing among options * within each question

Qn No.	Question	CL	CO
16	A) Examine the process of converting a binary number to its Excess-3 equivalent with an example. OR B) Examine how a 8 to 1 multiplexer works. Justify its operation with diagrams and truth table	AN	1, 4
17	A) Evaluate the behaviour of a JK flip-flop and justify how the race-around condition arises. OR B)	EV	3, 4

Qn No.	Question	CL	CO
	Assess the functionality of a 2-bit magnitude comparator in sorting applications. Compare its output logic with a 1-bit comparator and support your analysis with a truth table.		
18	A) Evaluate two different Boolean simplification methods — one using Boolean algebra and the other using Karnaugh maps — for the expression $F = A'B + AB' + AB$. Determine which is more efficient and explain why? OR B) Given the Boolean expression $F = (A + B)(C + D)$, assess whether implementing this function using AND, OR, and NOT gates or using only NAND gates would be more efficient in terms of gate count and circuit complexity. Justify your evaluation with reasoning.	EV	1, 2
19	A) Create a logic circuit for an XOR gate using only AND, OR, and NOT gates. Illustrate each step of the design, starting from the truth table to the final logic diagram. OR B) Create a T flip-flop and explain how it differs from other flip-flops like RS, D, and JK. Design the logic circuit and provide the truth table, followed by a timing diagram that illustrates the flip-flop's behavior with different clock inputs.	CR	2, 3