Eighth Semester B. Tech Degree Examination

(2013 Scheme)

13.802: Computer System Architecture

Marks: 100   **Time: 3 hrs**

PART-A

(Answer all questions. Each question carries 4 marks)

1. With the help of necessary figures, explain Flynn's classification of computer architectures.
2. Explain the routing mechanisms defined by a binary 3 cube using necessary diagrams.
3. With a neat diagram, explain the components of a backplane bus system.
4. Compare and contrast linear and non-linear pipelines.
5. How can the I/O operations bypassing cache result in cache coherence problem? Also, suggest a solution for preventing it.

(5 x 4 = 20)

PART-B

(Answer one full question from each module. Each question carries 20 marks)

Module-I

6. a. Explain the various dynamic interconnection networks.   (10)

   b. Explain the properties of an interconnection network.   (5)

   c. Identify the various dependences in the following:

P1: C = D x E

P2: M = G + C

P3: A = B + C

P4: C = L + M

P5: F = G / E   (5)

7. a. Explain the operational model of an SIMD supercomputer.   (5)

   b. Compare implicit and explicit forms of parallelism.   (5)

c. A workstation uses a 1.5 GHz processor with a claimed 1000 MIPS rating to execute a given program mix. Assume a one cycle delay for each memory access.

i. What is the effective CPI of this computer?

ii. Suppose the processor is being upgraded with a 3.0 GHz clock. However, even with faster cache two clock cycles are needed per memory access. If 30% of the instructions require one memory access and another 5% require two memory accesses per instruction, what is the performance of the upgraded processor with a compatible instruction set and equal instruction counts in the given program mix? (10)

Module-II

8. a. Explain the address translation mechanisms using Translation Lookaside Buffers and Page tables. (5)

b. Consider a two-level memory system with four page frames. A certain program generated the following page trace: 0, 1, 3, 6, 2, 4, 5, 2, 5, 0, 3, 1, 2, 5, 4, 1, 0.

   i. Find out the allotment of pages to the four page frames using LRU, OPT, and FIFO page replacement policies.

   ii. Compare the hit ratios associated with each of the three replacement policies. (15)

9. a. Compare and contrast CISC and RISC architectures. (4)

   b. With the help of a figure, explain memory hierarchy technology. (4)

   c. Low order memory interleaving supports block memory access, whereas high order memory interleaving does not. Justify the statement with the help of suitable diagrams. (12)

Module-III

10. Design a processor which can execute a series of instructions for computing two distinct functions – X and Y in an overlapped manner. The designed processor should involve three distinct stages – s1, s2, and s3 for performing the computations. Let the sequence of operations of the three stages be s1-s2-s3-s2-s3-s1-s3-s1 for computing X and s1-s3-s2-s3-s1-s3 for computing Y. Based on the design:

   a. Identify the forbidden and permissible latencies for both X and Y.

b. Depict the permissible state transitions among successive initiations of each of the functions X and Y.

c. Identify the simple latency cycles while computing the functions X and Y.

d. Find out the greedy cycles while computing X and Y.

e. What will be the maximum throughput of this pipeline?(20)

11. a. Consider the execution of a program of 15000 instructions by a linear pipeline processor with a clock rate of 25 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out of order sequence executions are ignored. Calculate the speed up, throughput, and efficiency.   (10)

   b. Explain the usage of CSA and CPA in an arithmetic pipeline with the help of an example.

(10)

Module-IV

12. a. Explain the different causes of cache coherence problem.   (8)

   b. Briefly explain the various snoopy bus protocols for enforcing cache coherence.   (12)

13. a. Explain the various vector access mechanisms.   (10)

   b. Write brief notes on data flow and hybrid architectures.   (10)

(20 x 4 = 80)