## SCHEME -2018

**III SEMESTER**  
**ELECTRONICS and COMMUNICATION ENGINEERING (T)**

<table>
<thead>
<tr>
<th>Course No</th>
<th>Name of subject</th>
<th>Credits</th>
<th>Weekly load, hours</th>
<th>Exam Duration Hrs</th>
<th>U E Max Marks</th>
<th>Total Marks</th>
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<tr>
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<td>L</td>
<td>T</td>
<td>D/P</td>
<td>CA Marks</td>
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<tr>
<td>18.301</td>
<td>Engineering Mathematics-II (T)</td>
<td>4</td>
<td>3</td>
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<tr>
<td>18.302</td>
<td>Signals &amp; Systems (T)</td>
<td>3</td>
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<tr>
<td>18.303</td>
<td>Network Analysis (T)</td>
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<td>3</td>
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<tr>
<td>18.304</td>
<td>Object Oriented Techniques (T)</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>-</td>
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<td>18.305</td>
<td>Electronic Circuits (T)</td>
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<td>3</td>
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<td>18.306</td>
<td>Logic Circuit Design (T)</td>
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<td>18.307</td>
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<td>18.308</td>
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18.301 ENGINEERING MATHEMATICS - II (T)

Teaching Scheme: 3(L) - 1(T) - 0(P)                                                                                   Credits: 4

Course Objective:
This course provides students a basic understanding of vector calculus, three dimensional geometry and Fourier transforms which are very useful in many engineering fields. Partial differential equations and its applications are also introduced as a part of this course.

Module – I


Module – II
Fourier Transforms: Fourier integral theorem (no proof) –Complex form of Fourier integrals Fourier integral representation of a function- Fourier transforms – Fourier sine and cosine transforms, inverse Fourier transforms, properties.


Module – III

Module – IV
Applications of Partial differential equations: Solution by separation of variables. One dimensional Wave and Heat equations (Derivation and solutions by separation of variables). Steady state condition in one dimensional heat equation. Boundary Value problems in one dimensional Wave and Heat Equations.

References:
**Internal Continuous Assessment** (Maximum Marks-50)
50% - Tests (minimum 2)
30% - Assignments (minimum 2) such as home work, problem solving, literature survey, seminar, term-project, software exercises, etc.
20% - Regularity in the class

University Examination Pattern:
Examination duration: 3 hours Maximum Total Marks: 100
The question paper shall consist of 2 parts.
Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.
Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

**Course Outcome**:
At the end of the course, the students will have the basic concepts of vector analysis, Fourier transforms, Three dimensional geometry and Partial differential equations which they can use later to solve problems related to engineering fields.
Course objectives:

To study the theory of signals and system. To study the interaction of signals with physical system. To study the properties of Fourier transform, Laplace transform, signal transform through linear system, relation between convolution and correlation of signals, sampling theorem and techniques, and transform analysis of LTI systems.

Module – I


Continuous Time LTI systems and Convolution Integral, Discrete Time LTI systems and linear convolution. Stability and causality of LTI systems. Correlation between signals, orthogonality of signals.

Module – II


Module – III

Sampling of continuous time signals, Sampling theorem for lowpass signals, aliasing. Sampling techniques, Ideal sampling, natural sampling and Flat-top sampling. Reconstruction, Interpolation formula. Sampling of bandpass signals.

Module – IV

Relation between DTFT and Z-Transform. Analysis of Discrete Time LTI systems using Z transforms and DTFT. Transfer function, Magnitude and phase response.

References


Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours  Maximum Total Marks: 100

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from module. Each question carries 20 marks.

Note: Question paper should contain minimum 60% and maximum 80% Problems and Analysis.

Course outcome:

After completion of the course students will have a good knowledge in signals, system and applications.
18.303 NETWORK ANALYSIS (T)

Teaching Scheme: 3(L) - 1(T) - 0(P)  
Credits: 3

Course Objectives:

To make the students capable of analyzing any given electrical network. To study the transient response of series and parallel A.C. Circuits. To study the concept of coupled circuits and two port networks. To make the students learn how to synthesize an electrical network from a given impedance / admittance function.

Module – I

Solution methods: Mesh and node analysis of network containing Independent and Dependent sources, Star-Delta transformation.
Network theorems: Thevenin’s theorem, Norton’s theorem, Superposition theorem, Reciprocity theorem, Millman’s theorem, Maximum Power Transfer theorem.

Module – II

S-Domain analysis: The concept of complex frequency, Network functions for the one port and two port - Poles and Zeros of network functions, Significance of Poles and Zeros, properties of driving point and transfer functions, Time domain response from pole zero plot.

Module – III

Parameters of two-port network: impedance, admittance, transmission and hybrid parameters, Interrelationship among parameters, Series and Parallel connections of Two Port network, Reciprocal and Symmetrical two ports. Characteristic impedance, Image Impedance and propagation constant. (Derivation not required)
Resonance: Series resonance, bandwidth, Q factor and Selectivity, Parallel resonance.
Module-IV
Coupled circuits: single tuned and double tuned circuits, dot convention, coefficient of
coupling, analysis of coupled circuits.
Network Synthesis: Introduction, Hurwitz Polynomial, Positive Real Functions. Properties and
Synthesis of R-L networks by the Foster and Cauer methods, Properties and Synthesis of R-C
networks by the Foster and Cauer methods.

References:
2. Sudhakar A. and S. P. Shyammohan, Circuits and Networks - Analysis and Synthesis, 3/e,
   TMH, 2006.

Internal Continuous Assessment (Maximum Marks-50)
50% - Tests (minimum 2)
30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey,
   seminar, term-project, software exercises, etc.
20% - Regularity in the class

University Examination Pattern:
Examination duration: 3 hours Maximum Total Marks: 100
The question paper shall consist of 2 parts.
Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are
compulsory. There should be at least two questions from each module and not more than
three questions from any module.
Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

Note: Question paper should contain minimum 60% and maximum 80% Problems and Analysis.

Course outcome:
At the end of the course students will be able analyze the electrical circuits and synthesize the electrical circuits.
18.304 Object Oriented Techniques(T)

Teaching Scheme: 3(L) - 1(T) - 0(P)  Credits: 3

Course Objectives:

- To provide strong foundation in programming and in C++

Module – I

Basic structure of a C++ program - Data types and Operators – Enumerated data types – Type conversion – Conditional statements and loops – Arrays (one and two dimensional) and strings – Functions - Recursive functions – Storage class specifiers.

Module – II

Pointers – Pointer to arrays and strings – Pointer to pointer – Array of pointers – Structures and Unions - new and delete operators for dynamic memory management

Classes and objects – private, public and protected variables - Constructors and Destructors – Array of class objects – Pointer and classes – ‘this’ pointer - Inline member Functions – Static Class Members.

Module – III

Function overloading, Operator overloading - Friend functions - Inheritance - Polymorphism - Virtual functions.

Data File Operations - Exception handling – Creating and Manipulating String Objects.

Module – IV

Data Structures: Linked lists (single) - basic operations - Stack and Queues - basic operations using arrays and linked lists.

Searching and Sorting – Linear Search and Binary Search - Bubble sort – Insertion sort – Selection sort.

References:


**Internal Continuous Assessment** *(Maximum Marks-50)*

- 50% - Tests (minimum 2)
- 30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.
- 20% - Regularity in the class

**University Examination Pattern:**

- Examination duration: 3 hours
- Maximum Total Marks: 100

The question paper shall consist of 2 parts.

**Part A (20 marks)** - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

**Part B (80 Marks)** - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

*Note:* Question paper should contain minimum 60% and maximum 80% Programming and Algorithms.

**Course Outcome:**

After successful completion of the course, the students will have the confidence and knowledge to write useful, complex and multifunction programs.
18.305 ELECTRONIC CIRCUITS (T)

Teaching Scheme: 3(L) - 1(T) - 0(P)    Credits: 4

Course Objectives:

- To study the working of various electronic circuits and their equivalent circuit.
- To analyze the different circuits and design the circuits using discrete components as per the specifications.

Module – I

Rectifiers: Half wave and full wave (including bridge rectifier), capacitor filter
Principle of operation of UJT and SCR.

DC analysis of BJTs - Transistor Biasing circuits, Q point, Bias stability, Stability factors, Concept of DC and AC Load line, RC coupled amplifier and its frequency response, effect of various components, Classification of BJT amplifiers, Small signal analysis of CE, CB, CC configurations using Small signal hybrid π model (gain, input and output impedance), cascade amplifier.

Module – II

High frequency equivalent circuits of BJTs, Analysis of high frequency response of CE, CB, CC Amplifiers, Miller effect, Wide Band amplifier: Broad banding techniques, low frequency and high frequency compensation, cascode amplifier.

MOSFET: Small signal equivalent circuits. Biasing of MOSFETs amplifiers, Classification of MOSFET amplifiers. DC Analysis of Single stage MOSFET amplifiers – small signal voltage and current gain, input and output impedance of CS amplifiers, MOSFET cascade amplifier.

Module – III

Feedback amplifiers (using BJT): The four basic feedback topologies, Feedback amplifier circuits in each feedback topologies (no analysis required).

Module – IV

Switching circuits: Simple sweep circuit, bootstrap sweep circuit, astable, monostable and bistable multivibrators.

Power amplifiers: Classification, transformer coupled class A power amplifier, push pull class B, and class AB power amplifiers, efficiency and distortion. Transformer-less power class B and class AB power amplifiers, class C power amplifier (no analysis required).

Power Supply: Zener diode regulator circuit, design and analysis of series voltage regulator (line and load regulation), Short circuit protection.

References:


Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)
30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.
20% - Regularity in the class

University Examination Pattern:

*Examination duration: 3 hours*  
*Maximum Total Marks: 100*

*The question paper shall consist of 2 parts.*

*Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.*
Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

Note: Question paper should contain minimum 60% and maximum 80% Analysis, Design and Problems.

Course Outcome:

At the end of the course, students will be able to analyse the different circuits. Also the students can design circuits using discrete electronic components.
18.306 LOGIC CIRCUIT DESIGN(T)

Teaching Scheme: 3(L) - 1(T) - 0(P)  
Credits: 3

Course Objectives:
- To study the concepts of number systems.
- To study the design of combination logic and sequential logic.
- To make the student familiar with internal structure of various digital logic families.
- To provide students the fundamentals to the design and analysis of digital circuits.

MODULE –I

Number systems- decimal, binary, octal, hexa decimal, base conversion. 1’s and 2’s complement, signed number representation. Binary arithmetic, binary subtraction using 2’s complement.

Binary codes (grey, BCD and Excess-3), Error detection and correcting codes: Parity(odd, even), Hamming code (7,4), Alphanumeric codes: ASCII. Logic expressions, Boolean laws, Duality, De Morgan's law, Logic functions and gates. Canonical forms: SOP, POS, Realisation of logic expressions using K-map (2,3,4 variables).

Design of combinational circuits – adder, subtractor, 4 bit adder/subtractor, BCD adder, MUX, DEMUX, Decoder, BCD to 7 segment decoder, Encoder, Priority encoder, Comparator (2/3 bits).

MODULE-II

Sequential circuits - latch, flip flop (SR, JK, T, D), master slave JK FF, conversion of FFs, excitation table and characteristic equations. Asynchronous and synchronous counter design, mod N counters, random sequence generator. Shift Registers - SIPO, SISO, PISO, PIPO, Shift registers with parallel LOAD/SHIFT.

Shift register counter - Ring Counter and Johnson Counter.

MODULE-III

Mealy and Moore models, state machine, notations, state diagram, state table, transition table, excitation table, state equations.

Construction of state diagram – up down counter, sequence detector.

Synchronous sequential circuit design - State equivalence.

State reduction – equivalence classes, implication chart.
MODULE-IV

Logic families and its characteristics: Logic levels, propagation delay, fan in, fan out, noise immunity, power dissipation, TTL subfamilies. NAND in TTL (totem pole, open collector and tri-state), CMOS: NAND, NOR, and NOT in CMOS, Comparison of logic families (TTL, ECL, CMOS) in terms of fan-in, fan-out, supply voltage, propagation delay, logic voltage and current levels, power dissipation and noise margin. Programmable Logic devices - ROM, PLA, PAL, implementation of simple circuits using PLA. Introduction to VHDL - VHDL description for basic gates, flip flops, Full adder, counters (Behavioural model only)

References:

Internal Continuous Assessment (Maximum Marks-50)
50% - Tests (minimum 2)
30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.
20% - Regularity in the class

University Examination Pattern:
Examination duration: 3 hours Maximum Total Marks: 100
The question paper shall consist of 2 parts.
Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.
Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.
Note: Question paper should contain minimum 50% and maximum 60% Analysis and Design.

Course Outcome:
The students will be familiar with different digital ICs and be able to design various digital circuits.
18.307 Electronic Devices & Circuits Lab (T)

Teaching Scheme: 0(L) - 0(T) - 3(P)  
Credits: 2

Course Objective:

- The purpose of the course is to enable students to have the practical knowledge of different semiconductor electronic devices.
- To study the specifications of devices and circuits.

List of Experiments:

1. VI Characteristics of rectifier and zener diodes
2. RC integrating and differentiating circuits (Transient analysis with different inputs and frequency response)
3. Clipping and clamping circuits (Transients and transfer characteristics)
4. Rectifiers half wave, full wave and bridge - with and without filter - ripple factor and regulation
5. Simple Zener voltage regulator (load and line regulation)
6. Characteristics of BJT in CE configuration and evaluation of parameters
7. Characteristics of MOSFET in CS configuration and evaluation of parameters
8. RC coupled CE amplifier - frequency response characteristics
9. MOSFET amplifier (CS) - frequency response characteristics
10. Cascade amplifier – gain and frequency response
11. Feedback amplifiers (current series, voltage series) - gain and frequency response
12. Oscillators –RC phaseshift, Wien bridge, Colpitt’s and Hartley
13. Power amplifiers (transformer less) - Class B and Class AB
14. Transistor series voltage regulator (load and line regulation)
15. Tuned amplifier - frequency response
16. Bootstrap sweep circuit

Internal Continuous Assessment (Maximum Marks-50)

- 40% - Test
- 40% - Class work and Fair Record
- 20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours  
Maximum Total Marks: 100

Questions based on the list of experiments prescribed.

Circuit and design - 25%,

Performance (Wiring, usage of equipment and trouble shooting) - 15%
Result - 35%; Viva voce - 25%

Candidate shall submit the certified fair record for endorsement by the external examiner.
Course Outcome:

On successful completion of the course, students will be able to know the working of semiconductor devices and design of circuits using these devices.
**18.308 OBJECT ORIENTED PROGRAMMING LAB (T)**

Teaching Scheme: 0(L) - 0(T) - 3(P)  
Credits: 2

**Course Objective:**

1. To acquaint students with Object Oriented concepts and terminology.  
2. To design and implement object oriented software to solve moderately complex problems.

**List of Experiments:**

Programming exercises based on the course Object Oriented Techniques. The exercises may include the following:-

1. Functions  
   a. Call by value, Call by reference  
   b. Function overloading  
   c. Default arguments

2. Classes and Objects  
   a. Classes with primitive data members, arrays  
   b. Classes with static data members and static member functions  
   c. Arrays of objects  
   d. Constructors and destructors - Parameterized constructor, copy constructor

3. Friend functions

4. Operator overloading  
   a. Overloading unary and binary operators

5. Inheritance  
   a. Single, multiple, multilevel and hierarchical inheritance  
   b. Virtual functions

6. File handling  
   a. Basic file operations

7. Stack and Queue using array

8. Searching (linear and binary)

9. Sorting (Bubble, insertion, selection)
Internal Continuous Assessment (Maximum Marks-50)
40% - Test
40% - Class work and Record (Up-to-date lab work, problem solving capability, keeping track of rough record and fair record, term projects, assignment, software/hardware exercises, etc.)
20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours Maximum Total Marks: 100

Questions based on the list of exercises prescribed.

Marks should be awarded as follows:

20% - Algorithm/Design

30% - Implementing / conducting the work assigned

25% - Output/Results and inference

25% - Viva voce

Candidate shall submit the certified fair record for endorsement by the external Examiner.

Course Outcome:

After successful completion of this course, students will be able to:

1. Familiarize classes and attributes in real world applications.
2. Perform programs using OOP concepts.
3. Distinguish the types of inheritance in different problems.
4. Perform applications by overloading operators and functions.