UNIVERSITY OF KERALA

B. TECH. DEGREE COURSE

(2018 SCHEME)

SYLLABUS FOR

III SEMESTER

ELECTRONICS and COMMUNICATION ENGINEERING

SCHEME -2018

III SEMESTER

ELECTRONICS and COMMUNICATION ENGINEERING (T)

Course No	Name of subject	Credits	Weekly load, hours			C A Marks	Exam Duration Hrs	U E Max Marks	Total Marks
			L	T	D/P				
18.301	Engineering Mathematics-II (T)	4	3	1	-	50	3	100	150
18.302	Signals & Systems (T)	3	3	1	-	50	3	100	150
18.303	Network Analysis (T)	3	3	1	-	50	3	100	150
18.304	Object Oriented Techniques(T)	3	2	1	-	50	3	100	150
18.305	Electronic Circuits (T)	4	3	1	-	50	3	100	150
18.306	Logic Circuit Design (T)	3	3	1		50	3	100	150
18.307	Electronic Devices& Circuits Lab (T)	2	-	-	3	50	3	100	150
18.308	Object oriented programming Lab(T)	2	-	-	3	50	3	100	150
	Total	**24**	**17**	**6**	**6**	**400**		**800**	**1200**

18.301 ENGINEERING MATHEMATICS - II (T)

Teaching Scheme: 3(L) - 1(T) - 0(P) **Credits: 4**

Course Objective :
This course provides students a basic understanding of vector calculus,three dimensional geometry and Fourier transforms which are very useful in many engineering fields. Partial differential equations and its applications are also introduced as a part of this course.

Module – I

Vector differentiation : Scalar and vector functions-differentiation of vector functions-velocity and acceleration - scalar and vector fields - vector differential operatorGradient-Physical interpretation of gradient - directional derivative – divergence - curl - identities involving (no proof) - irrotational and solenoidal fields - scalar potential.
Vector integration: Line, surface and volume integrals. Green's theorem in plane. Stoke's theorem and Gauss divergence theorem (no proof).

Module – II

Fourier Transforms: Fourier integral theorem (no proof) –Complex form of Fourier integralsFourier integral representation of a function- Fourier transforms – Fourier sine and cosine transforms, inverse Fourier transforms, properties.
Three dimensional geometry:Sphere-Equation of a sphere-Cone-Equation of a cone-Right circular cone-Cylinder-Equation of a cylinder-Right circular cylinder-Ellipsoid-Hyperboloid-Elliptic paraboloid-Hyperbolic paraboloid - Elliptic,Parabolic and Hyperbolic cylinders.

Module – III

Partial differential equations: Formation of PDE. Solution by direct integration. Solution of Lagrange's Linear equation. Nonlinear equations - Charpit method. Homogeneous PDE with constant coefficients.

Module – IV

Applications of Partial differential equations: Solution by separation of variables. One dimensional Wave and Heat equations (Derivation and solutions by separation of variables).Steady state condition in one dimensional heat equation. Boundary Value problems in one dimensional Wave and Heat Equations.

References :

1. Kreyszig E., Advanced Engineering Mathematics, 9/e, Wiley India, 2013.
2. Grewal B. S., Higher Engineering Mathematics, 13/e, Khanna Publications, 2012.
3. Ramana B.V., Higher Engineering Mathematics, Tata McGraw Hill,2012
4. Greenberg M. D., Advanced Engineering Mathematics, 2/e, Pearson, 1998.
5. Bali N. P. and M. Goyal, Engineering Mathematics, 7/e, Laxmi Publications, India,2012.
6. Koneru S. R., Engineering Mathematics, 2/e, Universities Press (India) Pvt. Ltd.,2012.
7.A.Gangadharan,Engineering Mathematics.

Internal Continuous Assessment (Maximum Marks-50)
50% - Tests (minimum 2)
30% - Assignments (minimum 2) such as home work, problem solving, literature survey, seminar, term-project, software exercises, etc.
20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours Maximum Total Marks: 100

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

Course Outcome **:**

At the end of the course, the students will have the basic concepts of vector analysis, Fourier transforms ,Three dimensional geometryand Partial differential equations which they can use later to solve problems related to engineering fields.

18.302 SIGNALS & SYSTEMS (T)

Teaching Scheme: 3(L) - 1(T) - 0(P) **Credits**: **3**

Course objectives:

To study the theory of signals and system. To study the interaction of signals with physical system. To study the properties of Fourier transform, Laplace transform, signal transform through linear system, relation between convolution and correlation of signals, sampling theorem and techniques, and transform analysis of LTI systems.

Module – I

Classification and Representation of Continuous time and Discrete time signals. Elementary signals, Signal operations. Continuous Time and Discrete Time Systems - Classification, Properties. Representation - Differential Equation representation of Continuous Time Systems. Difference Equation Representation of Discrete Systems.

Continuous Time LTI systems and Convolution Integral, Discrete Time LTI systems and linear convolution. Stability and causality of LTI systems. Correlation between signals, orthoganality of signals.

Module – II

Laplace Transform – ROC – Inverse transform – properties – unilateral Laplace Transform. Frequency Domain Representation of Continuous Time Signals- Continuous Time Fourier Series and its properties Convergence. Continuous Time Fourier Transform: Properties. Relation between Fourier and Laplace Transforms. Analysis of LTI systems using Laplace and Fourier Transforms. Concept of transfer function, Frequency response, Magnitude and phase response. Energy and power spectral densities. Condition for distortionless transmission.

Module – III

Sampling of continuous time signals, Sampling theorem for lowpass signals, aliasing. Sampling techniques, Ideal sampling, natural sampling and Flat-top sampling. Reconstruction, Interpolation formula. Sampling of bandpass signals.

Module – IV

Z transform – ROC – Inverse transform – properties –unilateral Z transform.

Frequency Domain Representation of Discrete Time Signals- Discrete Time Fourier Series and its properties, Discrete Time Fourier Transform (DTFT) and its properties.

Relation between DTFT and Z-Transform. Analysis of Discrete Time LTI systems using Z transforms and DTFT. Transfer function, Magnitude and phase response.

References

1. Oppenheim A. V. and A. Willsky, *Signals and Systems*, 2/e, PHI, 2009.
2. Rawat T. K., *Signals and Systems*, Oxford University Press, 2010.
3. Haykin S., *Signals & Systems*, 2/e, John Wiley, 2003.
4. Ziemer R. E., *Signals & Systems - Continuous and Discrete*, 4/e, Pearson, 2013.
5. Lathi B. P., *Principles of Signal Processing & Linear systems*, Oxford University Press, 2010.
6. Hsu H. P., *Signals and Systems*, 3/e, McGraw Hill, 2013.
7. Roberts M. J., *Signals and Systems*, 3/e, Tata McGraw Hill, 2003.
8. Kumar A., *Signals and Systems*, 3/e, PHI, 2013.
9. Chaparro L. F., *Signals and system using MATLAB*, Elsevier, 2011.
10. Yang W. W. *et. al.*, *Signals and Systems with MATLAB*, Springer, 2009.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from module. Each question carries 20 marks.

***Note:** Question paper should contain minimum 60% and maximum 80% Problems and Analysis.*

Course outcome:

After completion of the course students will have a good knowledge in signals, system and applications.

18.303 NETWORK ANALYSIS (T)

Teaching Scheme: 3(L) - 1(T) - 0(P) **Credits**: **3**

Course Objectives :

To make the students capable of analyzing any given electrical network. To study the transient response of series and parallel A.C. Circuits. To study the concept of coupled circuits and two port networks. To make the students learn how to synthesize an electrical network from a given impedance / admittance function.

Module – I

Network Topology, Network graphs, Trees, Incidence matrix, Tie-set matrix,Cut-set matrix and Dual networks.
Solution methods: Mesh and node analysis of network containing Independent and Dependent sources, Star-Delta transformation.
Network theorems: Thevenin's theorem, Norton's theorem, Superposition theorem, Reciprocity theorem, Millman's theorem, Maximum Power Transfer theorem.

Module – II

Laplace Transform in the Network Analysis: Initial and Final conditions, Transformed impedance and circuits, Transform of signal waveform. Transient analysis of RL, RC, and RLC networks with impulse, step and sinusoidal inputs. Analysis of networks with transformed impedances and dependent sources.
S-Domain analysis: The concept of complex frequency, Network functions for the one port and two port - Poles and Zeros of network functions, Significance of Poles and Zeros, properties of driving point and transfer functions, Time domain response from pole zero plot.

Module – III

Parameters of two-port network: impedance, admittance, transmission and hybrid parameters, Interrelationship among parameters, Series and Parallel connections of Two Port network, Reciprocal and Symmetrical two ports. Characteristic impedance, Image Impedance and propagation constant. (Derivation not required)
Resonance: Series resonance, bandwidth, Q factor and Selectivity, Parallel resonance.

Module-IV

Coupled circuits: single tuned and double tuned circuits, dot convention, coefficient of coupling, analysis of coupled circuits.

Network Synthesis:Introduction,Hurwitz Polynomial, Positive Real Functions. Properties and Synthesis of R-L networks by the Foster and Cauer methods, Properties and Synthesis of R-C networks by the Foster and Cauer methods.

References:

1. Valkenburg V., *Network Analysis*, 3/e, PHI, 2011.

2. Sudhakar A. and S. P. Shyammohan, *Circuits and Networks- Analysis* and Synthesis, 3/e, TMH, 2006.

3. Choudhary R., *Networks and Systems,* 2/e, New Age International, 2013.

4. Kuo F. F., *Network Analysis and Synthesis,* 2/e, Wiley India, 2012.

5. Gupta B. R. and V. Singhal, *Fundamentals of Electrical Networks*, S. Chand, 2009.

6. Sinha U., *Network Analysis & Synthesis*, 7/e, Satya Prakashan, 2012.

7. Ghosh S., *Network Theory – Analysis & Synthesis,* PHI, 2013.

8. Somanathan Nair B., *Network Analysis and Synthesis*, Elsevier, 2012.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

Note: *Question paper should contain minimum 60% and maximum 80% Problems and Analysis.*

Course outcome:

At *the end of the course students will be able analyze the electrical circuits and synthesize the electrical circuits.*

18.304 Object Oriented Techniques(T)

Teaching Scheme: 3(L) - 1(T) - 0(P) **Credits: 3**

Course Objectives:

- *To provide strong foundation in programming and in C++*

Module – I

Basic stricture of a C++ program - Data types and Operators – Enumerated data types – Type conversion – Conditional statements and loops – Arrays (one and two dimensional) and strings – Functions - Recursive functions – Storage class specifiers .

Module – II

Pointers – Pointer to arrays and strings – Pointer to pointer – Array of pointers – Structures and Unions - new and delete operators for dynamic memory management

Classes and objects – private, public and protected variables - Constructors and Destructors – Array of class objects – Pointer and classes – 'this' pointer - Inline member Functions – Static Class Members.

Module – III

Function overloading, Operator overloading - Friend functions - Inheritance - Polymorphism - Virtual functions.

Data File Operations - Exception handling – Creating and Manipulating String Objects.

Module – IV

Data Structures: Linked lists (single) - basic operations - Stack and Queues - basic operations using arrays and linked lists.

Searching and Sorting – Linear Search and Binary Search - Bubble sort – Insertion sort – Selection sort.

References:

1. Stroustrup B., *The C++ Programming Language*, 4/e, Addison-Wesley, 2013.
2. Balagurusamy E., *Object Oriented Programming with C++*, 6/e, Tata McGraw Hill, 2013.
3. Aho A. V., J. E. Hopcroft and J. D. Ullman, *Data Structures and Algorithms*, Pearson, 2005

4. Ravichandran D., *Programming with C++*, 3/e, Tata McGraw Hill, 2011.
5. Kanetkar Y*., Let us C++,* BPB Publications, 2003.
6. Eckel B., *Thinking in C++*, *Vol.* I, 2/e, Prentice Hall, 2000.
7. Eckel B. and C. Allison, *Thinking in C++*, *Vol.* II, Prentice Hall, 2004.
8. Samanta D., *Classic Data Structures*, Prentice Hall, 2006.
9. Sagar A. D., *Expert Data Structures using C/C++,* BPB Publications, 2009.
10. Kanetkar Y., *Data Structures through C++,* BPB Publications, 2003.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

***Note:** Question paper should contain minimum 60% and maximum 80% Programming and Algorithms.*

Course Outcome:

After successful completion of the course, the students will have the confidence and knowledge to write useful, complex and multifunction programs.

18.305 ELECTRONIC CIRCUITS (T)

Teaching Scheme: 3(L) - 1(T) - 0(P) **Credits**: **4**

Course Objectives :

- *To study the working of various electronic circuits and their equivalent circuit.*
- *To analyze the different circuits and design the circuits using discrete components as per the specifications.*

Module – I

Rectifiers: Half wave and full wave(including bridge rectifier), capacitor filter
RC Circuits: RC Low pass and High pass filter and its frequency response, Differentiator, Integrator. Diode Circuits: clippers, clampers.
Principle of operation of UJT and SCR.

DC analysis of BJTs - Transistor Biasing circuits, Q point, Bias stability, Stability factors, Concept of DC and AC Load line, RC coupled amplifier and its frequency response, effect of various components, Classification of BJT amplifiers, Small signal analysis of CE, CB, CC configurations using Small signal hybrid π model (gain, input and output impedance), cascade amplier.

Module – II

High frequency equivalent circuits of BJTs, Analysis of high frequency response of CE, CB, CC Amplifiers, Miller effect, Wide Band amplifier: Broad banding techniques, low frequency and high frequency compensation, cascode amplifier.

MOSFET: Small signal equivalent circuits. Biasing of MOSFETs amplifiers, Classification of MOSFET amplifiers. DC Analysis of Single stage MOSFET amplifiers – small signal voltage and current gain, input and output impedance of CS amplifiers, MOSFET cascade amplifier.

Module – III

Feedback amplifiers (using BJT): The four basic feedback topologies, Feedback amplifier circuits in each feedback topologies (no analysis required).

Oscillators (using BJT): Barkhausen criterion, Analysis of RC phase shift and Wein Bridge oscillator. Working of Hartley, Colpitts and Crystal oscillators. Tuned amplifiers, synchronous and stagger tuning.

Module – IV

Switching circuits : Simple sweep circuit, bootstrap sweep circuit, astable , monostable and bistable multivibrators.

Power amplifiers: Classification, transformer coupled class A power amplifier, push pull class B, and class AB power amplifiers, efficiency and distortion. Transformer-less power class B and class AB power amplifiers, class C power amplifier (no analysis required).

Power Supply: Zener diode regulator circuit, design and analysis of series voltage regulator (line and load regulation), Short circuit protection.

References:

1. Sedra A. S. and K. C. Smith, *Microelectronic Circuits*, 6/e, Oxford University Press, 2013 .

2. Neamen D., *Electronic Circuit Analysis and Design*, 3/e, TMH, 2006

3. Spencer R. R. and M. S. Ghausi, *Introduction to Electronic Circuit Design,* Pearson, 2003.

4. Boylestad R. L. and L. Nashelsky, *Electronic Devices and Circuit Theory*, 10/e, Pearson, 2009.

5. Millman J. and C. Halkias, *Integrated Electronics*, 2/e, TMH, 2010.

6. Howe R. and C. Sodini**,** *Microelectronics: An Integrated Approach,* Pearson, 2008.

7. Singh R. and B. P. Singh, *Electronic Devices and Circuits*, 2/e, Pearson, 2013.

8. Gopakumar K., *Design and Analysis of Electronic Circuits*, 2/e, Phasor Books, 2008.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)
30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.
20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

Note: *Question paper should contain minimum 60% and maximum 80% Analysis, Design and Problems.*

Course Outcome:

At the end of the course, students will be able to analyse the different circuits .Also the students can design circuits using discrete electronic components.

18.306 LOGIC CIRCUIT DESIGN(T)

Teaching Scheme: **3(L) - 1(T) - 0(P)** **Credits**: **3**

Course Objectives :

- To study the concepts of number systems.
- To study the design of combination logic and sequential logic.
- To make the student familiar with internal structure of various digital logic families.
- To provide students the fundamentals to the design and analysis of digital circuits.

MODULE –I

Number systems- decimal, binary, octal, hexa decimal, base conversion.1's and 2's complement, signed number representation. Binary arithmetic, binary subtraction using 2's complement

Binary codes (grey, BCD and Excess-3), Error detection and correcting codes: Parity(odd, even), Hamming code (7,4), Alphanumeric codes : ASCII .Logic expressions, Boolean laws, Duality, De Morgan's law, Logic functions and gates. Canonical forms: SOP, POS, Realisation of logic expressions using K-map (2,3,4 variables).

Design of combinational circuits – adder, subtractor, 4 bit adder/subtractor, BCD adder, MUX, DEMUX, Decoder,BCD to 7 segment decoder, Encoder, Priority encoder, Comparator (2/3 bits).

MODULE-II

Sequential circuits - latch, flip flop (SR, JK, T, D), master slave JK FF, conversion of FFs, excitation table and characteristic equations. Asynchronous and synchronous counter design, mod N counters, random sequence generator. Shift Registers - SIPO, SISO, PISO, PIPO, Shift registers with parallel LOAD/SHIFT

Shift register counter - Ring Counter and Johnson Counter.

MODULE-III

Mealy and Moore models, state machine ,notations, state diagram, state table, transition table, excitation table, state equations

Construction of state diagram – up down counter, sequence detector

Synchronous sequential circuit design - State equivalence

State reduction – equivalence classes, implication chart.

MODULE-IV

Logic families and its characteristics: Logic levels, propagation delay, fan in, fan out, noise immunity , power dissipation, TTL subfamilies.NAND in TTL (totem pole, open collector and tri-state), CMOS:NAND, NOR, and NOT in CMOS, Comparison of logic families (TTL,ECL,CMOS) in terms of fan-in, fan-out, supply voltage, propagation delay, logic voltage and current levels, power dissipation and noise margin.Programmable Logic devices - ROM, PLA, PAL, implementation of simple circuits using PLA. Introduction to VHDL- VHDL description for basic gates, flip flops, Full adder, counters (Behavioural model only)

References:

1. Roth (Jr.) C. H., Fundamentals of Logic Design, 6/e, Cengage Learning, 2010.
2. Anand Kumar A., Fundamentals of Digital Circuits, 2/e, PHI, 2012
3. Yarbrough J. M., Digital logic- Application and Design, Thomson Learning, 2006.
4. Wakerly J., Digital Design Principles and Practice, 4/e, Pearson, 2012.
5. Floyd T. L., Digital Fundamentals, 10/e, Pearson, 2011.
6. Mano M. M. And M. D. Ciletti, Digital Design, 4/e, Pearson, 2009.
7. DeMessa T. A., Z. Ciecone, Digital Integrated Circuits, Wiley India, 2007.
8. Ghoshal S., Digital Electronics, Cengage Learning, 2012.
9. Somanathan Nair B., Digital Electronics and Logic Design, 2/e, PHI, 2013.

Internal Continuous Assessment (Maximum Marks-50)

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours Maximum Total Marks: 100

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

Note: Question paper should contain minimum 50% and maximum 60% Analysis and Design.

Course Outcome:

The students will be familiar with different digital ICs and be able to design various digital circuits.

18.307 Electronic Devices & Circuits Lab (T)

Teaching Scheme: 0(L) - 0(T) - 3(P) **Credits**: **2**

Course Objective:

- *The purpose of the course is to enable students to have the practical knowledge of different semiconductor electronic devices.*
- *To study the specifications of devices and circuits.*

List of Experiments:

1. VI Characteristics of rectifier and zener diodes
2. RC integrating and differentiating circuits (Transient analysis with different inputs and frequency response)
3. Clipping and clamping circuits (Transients and transfer characteristics)
4. Rectifiers half wave, full wave and bridge -with and without filter- ripple factor and regulation
5. Simple Zener voltage regulator (load and line regulation)
6. Characteristics of BJT in CE configuration and evaluation of parameters
7. Characteristics of MOSFET in CS configuration and evaluation of parameters
8. RC coupled CE amplifier - frequency response characteristics
9. MOSFET amplifier (CS) - frequency response characteristics
10. Cascade amplifier – gain and frequency response
11. Feedback amplifiers (current series, voltage series) - gain and frequency response
12. Oscillators –RC phaseshift, Wien bridge, Colpitt's and Hartley
13. Power amplifiers (transformer less) - Class B and Class AB
14. Transistor series voltage regulator (load and line regulation)
15. Tuned amplifier - frequency response
16. Bootstrap sweep circuit

Internal Continuous Assessment *(Maximum Marks-50)*

40% - Test

40% - Class work and Fair Record

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

Questions based on the list of experiments prescribed.

Circuit and design - 25%,

Performance (Wiring, usage of equipment and trouble shooting) - 15%
Result - 35% ; Viva voce - 25%

Candidate shall submit the certified fair record for endorsement by the external examiner.

Course Outcome:

On successful completion of the course, students will be able to know the working of semiconductor devices and design of circuits using these devices.

18.308 OBJECT ORIENTED PROGRAMMING LAB (T)

Teaching Scheme: 0(L) - 0(T) - 3(P) **Credits**: **2**

Course Objective:

1 .To acquaint students with Object Oriented concepts and terminology.
2. To design and implement object oriented software to solve moderately complex problems.

List of Experiments:

Programming exercises based on the course Object Oriented Techniques. The exercises may include the following:-

1. Functions
    a. Call by value, Call by reference
    b. Function overloading
    c. Default arguments

2. Classes and Objects
    a. Classes with primitive data members, arrays
    b. Classes with static data members and static member functions
    c. Arrays of objects
    d. Constructors and destructors - Parameterized constructor, copy constructor

3. Friend functions

4. Operator overloading
    a. Overloading unary and binary operators
5. Inheritance
    a. Single, multiple, multilevel and hierarchical inheritance
    b. Virtual functions
6. File handling
    a. Basic file operations
7. Stack and Queue using array
8. Searching (linear and binary)
9. Sorting (Bubble, insertion, selection)

Internal Continuous Assessment (Maximum Marks-50)

40% - Test

40% - Class work and Record (Up-to-date lab work, problem solving capability, keeping track of rough record and fair record, term projects, assignment,
software/hardware exercises, etc.)

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours Maximum Total Marks: 100

Questions based on the list of exercises prescribed.

Marks should be awarded as follows:

20% - Algorithm/Design

30% - Implementing / conducting the work assigned

25% - Output/Results and inference

25% - Viva voce

Candidate shall submit the certified fair record for endorsement by the external Examiner.

Course Outcome:

After successful completion of this course, students will be able to:

1. Familiarize classes and attributes in real world applications.
2. Perform programs using OOP concepts.
3. Distinguish the types of inheritance in different problems.
4. Perform applications by overloading operators and functions.