# M.Tech. Programme

**Electronics and Communication – Embedded Systems**

## Curriculum and Scheme of Examinations

### SEMESTER-I

<table>
<thead>
<tr>
<th>Code</th>
<th>Name of the Subject</th>
<th>Credits</th>
<th>Hours/week</th>
<th>Exam Duration (hrs)</th>
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<td>TEM1001</td>
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<td>Of the 40 marks of internal assessment 25 marks for test and 15 marks for assignment. End semester exam is conducted by the University</td>
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** Students can select a subject from the subjects listed under stream/department electives for the second semester as advised by the course coordinator.
**STREAM ELECTIVES OFFERED IN EMBEDDED SYSTEM FOR SEMESTER II**

**Stream Elective I**
- TES 2001 DSP For Embedded Systems
- TES 2002 Designing With ASICS
- TES 2003 Embedded Linux
- TES 2004 Embedded Networking
- TES 2005 VLSI Digital Signal Processing

**Stream Elective II**
- TES 2006 Advanced DSP With FPGA
- TES 2007 Embedded Communication Software Design
- TES 2008 Digital Design For Testing & Testability
- TES 2009 Software Radio
- TES 2010 Intelligent Embedded Systems

**Department Electives Offered For Semester II**
- TED 2001 Cryptography & Network Security
- TED 2002 Advanced Signal Processing Methods
- TED 2003 Image Processing With Digital Signal Processors
- TED 2004 Robotics and Machine Vision
- TED 2005 Electronic Product Design
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<tr>
<th>Code</th>
<th>Name of the Subject</th>
<th>Credits</th>
<th>Hours/week</th>
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Of the 40 marks of internal assessment 25 marks for test and 15 marks for assignment. End Semester Exam is conducted by the Individual Institutions.

Do

Do

No End semester Examination

6 hrs of departmental assistance work

** Students can select a subject from the subjects listed under Stream Electives III and IV as advised by the course coordinator.

* Students can select a subject from the subjects listed under Non-Dept. (Interdisciplinary) Elective as advised by the course coordinator.

STREAM ELECTIVES OFFERED IN EMBEDDED SYSTEM FOR SEMESTER III

Stream Elective III

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<td>TES 3001</td>
<td>Mixed Signal Modeling</td>
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<td>TES 3002</td>
<td>Low Power VLSI Design</td>
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<td>TES 3003</td>
<td>Cloud Computing</td>
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<td>TES 3004</td>
<td>Embedded System Design With ARM</td>
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<tr>
<td>TES 3005</td>
<td>Soft Computing Techniques</td>
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Stream Elective IV

TES 3006  Embedded Control Systems
TES 3007  Algorithm For VLSI Design
TES 3008  Hardware Software Co-design
TES 3009  Fault Tolerant Computing
TES 3010  Adhoc Networks
### SEMESTER-IV

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<th>Code</th>
<th>Name of the Subject</th>
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TEM 1001  GRAPH THEORY

Structure of the Course

Lecture : 3 hrs/ Week  
Internal Continuous Assessment : 40 Marks
End Semester Examination : 60 Marks

Credits: 3

Course Objectives

- Learn the essentials of Graph Theory
- Learn the important applications of graph theory in digital VLSI system design

Learning Outcomes

- Ability to identify appropriate algorithms for circuit minimization and optimization
- Ability to apply graph theoretic algorithms in computer aided design of VLSI circuits

Module I


Module II

Planar graphs- Kuratowski’s two graphs-dual graphs-matrix representation of graphs-incidence matrix-circuit matrix-cut set matrix-path matrix-colourability-chromatic number-matchings-coverings and independence-the four colour problem-directed graphs-digraphs- digraphs and matrices-tournaments

Module III

Computer representation of graph-basic algorithms-shortest path algorithms-graphs in switching and coding theory-prefix codes-Huffman coding-Fault detection in combinational switching circuits-Algorithms for generating a fault matrix-procedure for detection of faults

References

1. NarsinghDeo, Graph Theory: with applications to engineering and science, Prentice Hall India,2004
3. Frank Harary, Graph Theory, Narosa publishing house, New Delhi, 2001
Structure of Question Paper
There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TEC 1001       ADVANCED LOGIC SYSTEM DESIGN

Structure of the Course

Lecture : 3 hrs/ Week
Internal Continuous Assessment : 40 Marks
End Semester Examination : 60 Marks

Credits: 3

Course Objectives

• Define a hardware design utilizing the three basic VHDL modeling styles: data flow, structural, and behavioral.
• Design and implement a complex state machine utilizing VHDL.
• Describe the fundamental architecture of a standard Field Programmable Logic Device

Learning Outcomes

• Thorough understanding of VHDL
• Ability to design, develop, test and document complete FPGA based designs

Module I
Introduction to VHDL- Karnaugh map-Tabular and computer aided minimization procedures-Multilevel gate circuits- Arithmetic circuits-design of arithmetic circuits using VHDL-Combinational building blocks-multiplexers-decoders-priority encoders- code converters-VHDL for combinational circuits

Module II
Synchronous sequential design-basic design steps-Finite State Machines(FSM)-Moore model-Mealy model-state machines in VHDL-VHDL test benches for state machines-VHDL models of sequential logic blocks-latches-flip flops-registers and shift registers-counters-memory-sequential multipliers-Linked state machines-state minimization-FSM as an arbiter circuit-analysis of synchronous sequential circuits-Algorithmic State Machine(ASM)-synthesis of ASM charts-analysis and synthesis of asynchronous sequential circuits-state reduction and state assignment-Races and Hazards-Types of hazards-Hazards in combinational circuit

Module III
References:


Structure of Question Paper

*There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.*
Structure of the Course

Lecture: 3 hrs/ Week  
Internal Continuous Assessment: 40 Marks 
End Semester Examination: 60 Marks

Course Objectives

- Understand current applications, trends and new directions in embedded systems
- Understand the performance metrics for an embedded system.
- The understanding of embedded systems using modular design and abstraction.

Learning Outcomes

- Thorough understanding of the basic embedded system concepts
- Ability to assemble and program an embedded system

Module I: Introduction To Embedded Systems

Embedded systems and their characteristics - Special challenges with embedded systems - Microcontrollers and other target architectures - Digital Signal processors-FPGAs-Intellectual property SoC Cores-embedded system architecture-embedded system model-overview of networking and programming language standards- Real time concepts-embedded system examples - A sample embedded system with multiple standards-the digital TV

Module II: Embedded Hardware


Module III: Embedded Programming Concepts

Data structures, Sample data types, complex data types-Conditional statements-loops-other flow control statements-Communication protocols-simple data broadcast-event driven single broadcast Event driven multi element transfers- state machines-data indexed state machines-execution indexed state machines-hybrid state machines-Multitasking-context switching-communications-managing priorities-timing control-state machine multitasking.
References:


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40 % Theory.
TEC 1003 VLSI SYSTEM DESIGN

Structure of the Course

Lecture: 3 hrs/ Week
Internal Continuous Assessment: 40 Marks
End Semester Examination: 60 Marks

Credits: 3

Course Objectives

• The course is designed to introduce the fundamental concepts of CMOS circuit design.
• Gives an understanding of the different design steps required to carry out a complete digital VLSI design in silicon.
• To have an understanding of various CMOS logic structures and to design functional subsystem units such as adders, multipliers, comparators, ALUs, shifters and memories such as SRAM, DRAM, and ROM.

Learning Outcomes

• Students will be able to use mathematical methods and circuit analysis of CMOS digital electronics circuits.
• Students will have an understanding of the different design steps required to carry out a complete digital VLSI design in silicon.
• Be able to complete a VLSI Design project having a set of objectives and design constraints.

Module I: Introduction to CMOS circuits
MOS Transistors- MOS transistor switches- CMOS logic- Inverter- NAND gate- NOR gate- compound gates- Multiplexers-Memory-Latches and Registers-circuit and system representations-Introduction to MOS transistor theory- MOS device design equations- second order effects-MOS models—small signal AC characteristics-CMOS inverter-DC characteristics- static load MOS inverters-Differential inverter-Transmission gate –Tristate Inverter-Bipolar devices- BiCMOS Inverters

Module II: Circuit characterization and performance estimation
Module III: CMOS logic structures and subsystem design

CMOS complimentary logic-BiCMOS logic- Pseudo- nMOS LOGIC-Dynamic CMOS LOGIC-Clocked CMOS logic-pass transistor logic-CMOS Domino logic-cascade voltage switch logic-SFPL logic- Data path operations- Single-bit adders-Bit parallel adder-Bit serial adders-carry save adders-transmission gate adders- carry-look ahead adders-carry select adders-parity generators-one/zerodetectors-comparators-counters-ALUs-Shifters-Multiplication-Array multiplication- Wallace Tree Multiplication-Memory elements-SRAM-Memory cell read/write operation-DRAM-Sub array architectures-Read-only memory-Content Addressable Memory-FSM-Design procedure

References:

4. John P. Uyemura,” Introduction to VLSI circuits and systems”, Wiley India (P) Limited.

Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TEC 1004 EMBEDDED PROCESORS

Structure of the Course

Lecture: 3 hrs/ Week Credits: 3
Internal Continuous Assessment: 40 Marks
End Semester Examination: 60 Marks

Course Objectives

• To learn the architecture, programming, interfacing of certain 8 bit and 32 bit microcontrollers
• To design and develop microcontroller based embedded systems

Learning Outcomes

• Familiarity with the architecture of the various microcontrollers
• Ability to write assembly language programs for application development using microcontrollers.
• Ability to develop an independent embedded system

Module I: Architecture of microcontrollers
Architecture of a microcontroller-Intel 8051 architecture-instruction set-addressing modes-Real time control: interrupts-interrupt handling in an MCU-interrupt structure in 8051-timers-programmable timers in MCUs-free running counter and real time control-real time clock interrupts-software timers-interrupt interval and density constraints.

Module II: Peripherals and interfacing
8051Peripherals and interfacing-serial UART and USART communication interface-Parallel I/O ports interface -DMA controller-programmable interrupt controller-ADC/DAC interfacing-Inter Integrated Circuit interfacing-interfacing of analog and digital systems-8051 interfacing with external memory, sensors, and motor interface-assembly language programming-programming the ports, timers, interrupts, read and write to external memory.

Module III: Arm an advanced microcontroller
32-bit ARM family-Processor and CPU cores –The ARM instruction set architecture-ARM pipeline-ARM assembly language programming-ARM organization and implementation-The ARM instruction set-The thumb instruction set-ARM9-ARM Cortex M3-Thumb2-Exceptions in ARM-Embedded ARM applications

References

2. Han-Way Huang, “Embedded system design using C8051”, Cengage Learning, 2011
5. Andrew N. Sloss, Dominic Symes, Chris Wright, “ARM System Developer’s guide”, Morgan Kaufman, 2005

Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TEC 1005 EMBEDDED SYSTEMS PROGRAMMING

Structure of the Course

Lecture: 3 hrs/ Week  Credits: 3
Internal Continuous Assessment: 40 Marks
End Semester Examination: 60 Marks

Course Objectives

• Understand the embedded programming concepts
• Familiarize with the use of C and Java for embedded system programming

Learning Outcomes

• Ability to program embedded systems using C and Java

Module I: Embedded C programming
Review of data types – scalar types-Primitive types-Enumerated types-Subranges, Structure types-character strings – arrays- Functions, Introduction to Embedded C-Introduction, Data types Bit manipulation, Interfacing C with Assembly. Embedded programming issues – Reentrance, Portability, Optimizing and testing embedded C programs.

Module II: Embedded applications using data structures
Linear data structures– Stacks and Queues, Implementation of stacks and Queues- Linked List - Implementation of linked list, Sorting, Searching, Insertion and Deletion, Nonlinear structures.

Module III: Embedded Java
Introduction to Object Oriented Concepts: Core Java/Java Core- Java buzzwords, Overview of Java programming, Data types, variables and arrays, Operators, Control statements. Embedded Java – Understanding J2ME, Connected Device configuration, Connected Limited device configuration, Profiles, Anatomy of MIDP applications, Advantages of MIDP

References:


Structure of Question Paper
There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40 % Theory.
Structure of the Course

Lecture: 2 hrs/Week
Internal Continuous Assessment: 100 Marks

Course Objectives

- Understand the embedded programming concepts
- Familiarize with the use of Embedded C and Java for embedded system programming

Learning Outcomes

- Ability to program embedded systems using C and Java

I 8051 Assembly and C programming

1. Programming timers & Counters
2. Programming Serial Port
3. Interrupt Programming in assembly & C
4. LCD and keyboard interfacing
5. Interfacing ADC, DAC, Sensors, external Memory
6. Interfacing 8255 and DS12887
7. Motor control: relay, PWM, DC and Stepper motors
8. I2C interface and software protocol

II ARM Programming

1. Communicate with PC via UART port and USB port.
2. Accessing 7 – Segment display through I2C.
3. Interfacing Temperature sensor, stepper motor, TFT, and Ethernet controller.
5. Interfacing Zigbee module and establish Zigbee network.
6. Implementing CAN network.
7. Configuring RTC to Clock and Alarm operations.
8. Perform ADC operation and plot the values in Graphical LCD.

III VHDL

1. Design and Implementation of Arithmetic circuits
2. Multiplexer, De-multiplexer
3. Encoder, 4:16 Decoder using 3:8 decoder, priority encoder
4. Four Bit comparator using one bit comparator
5. Unsigned and Signed Multiplier/Divider
6. (a) Flip-Flop with synchronous and Asynchronous Reset
   (b) D-FF, SR-FF, JK FF, Master slave D-FF
7. 4 Bit UP/DOWN counter, BCD Counter
8. Universal shift registers
10. serial adder using FSM approach
11. Design and implementation of a simple Microprocessor
12. Vending Machine Controller using FSM approach
Structure of the Course

Lecture : 2 hrs/ Week
Internal Continuous Assessment : 100 Marks
Credits : 2

The student is expected to present a seminar in one of the current topics in embedded systems and related areas. The student will undertake a detailed study based on current published papers, journals, books on the chosen subject and submit seminar report at the end of the semester.

Marks: Seminar Report Evaluation : 50 Marks
Seminar Presentation : 50 Marks
**Structure of the Course**

<table>
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<th>Lecture</th>
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<td>End Semester Examination</td>
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**Course Objectives**

- Familiarize the design of embedded computer system hardware
- Design, implement, and debug multi-threaded application software that operates under real-time constraints on embedded computer systems

**Learning Outcomes**

- Identification and synthesis of solutions for embedded system problems.
- Ability to design, execute and evaluate experiments on embedded platforms.

**Module I: System specification and specification languages**


**Module II: System verification and partitioning**

Translation to VHDL: state transitions-message passing communication-concurrency-exception handling-program-state machine to tasks- System partitioning-Structural versus functional partitioning, positioning issues-basic partitioning algorithms-Functional partitioning of Hardware-Hardware/Software partitioning algorithms-functional partitioning for algorithms

**Module III: Design quality estimation and specification refinement**

Quality metrics-hardware estimation-software estimation-Estimation techniques in system level tools-Specification refinement-refining variable groups-resolving access conflicts-refining incompatible interfaces-refining hardware/software interfaces-conceptualization environment for system design- design examples: Answering machine-ITVP-MP3 decoder

**References**


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
Structure of the Course

Lecture : 3 hrs/ Week
Internal Continuous Assessment : 40 Marks
End Semester Examination : 60 Marks

Course Objectives

• Understand the basics of RTOS
• Familiarize various Real time operating systems available and their use in embedded systems

Learning Outcomes

• Able to summarize the basic properties of a real-time operating system
• Ability to apply RTOS concepts for solving multi tasking embedded applications

Module I: Introduction to real time operating systems
Review of operating systems–real time embedded systems and real time operating systems-basics of developing for embedded systems-embedded system initialization-Defining RTOS-Tasks-Typical task scheduling and operations-synchronization, communication and concurrency-semaphores-typical semaphore operations and use-message queues-message queue states, content and storage-typical message queue operations and use-pipes-event registers-signals-condition variables-other RTOS services. Survey of Real time operating systems-POSIX-PSOS-VxWorks-QNX-MicroC/OS-II-RT Linux-Lynx-WindowsCE

Module II: Hardware and the RTOS
Exceptions and interrupts-Applications of exceptions and interrupts-timer and timer services-real time clocks and systems clocks-programmable interval timers-soft timers and timer related operations-I/O subsystem-Dynamic memory allocation-fixed size memory management-blocking and nonblocking memory functions-hardware memory management units-Synchronization and communication-common design problems.

Module III: Modern real time kernels and operating systems
POSIX-POSIX mutexes and condition variables-POSIX semaphores-POSIX messages-real time POSIX signals-clocks and timers-Asynchronous I/O-POSIX memory tasking-RTX51-RTX51 functions-preemptive scheduling in RTX51-C functions in RTX51-Use of Signal functions of RTX51 in design-Use of RTX51 in the design of traffic light control system and vending machine-Real Time Software components-TI DSP/BIOS and SYS/BIOS as scalable real time kernels-Use of DSP/BIOS in the design of an edge detection system.
References:


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40 % Theory.
Structure of the Course

Lecture : 2 hrs/ Week  Credits : 2
Internal Continuous Assessment : 40 Marks
End Semester Examination : 60 Marks

Course Objective

- To formulate a viable research question
- To distinguish probabilistic from deterministic explanations
- To analyze the benefits and drawbacks of different methodologies
- To understand how to prepare and execute a feasible research project

Learning Outcomes

Students are exposed to the research concepts in terms of identifying the research problem, collecting relevant data pertaining to the problem, to carry out the research and writing research papers/thesis/dissertation.

Module I

Introduction to Research Methodology - Objectives and types of research: Motivation towards research - Research methods vs. Methodology. Type of research: Descriptive vs. Analytical, Applied vs. Fundamental, Quantitative vs. Qualitative, and Conceptual vs. Empirical. Research Formulation - Defining and formulating the research problem - Selecting the problem - Necessity of defining the problem - Importance of literature review in defining a problem. Literature review: Primary and secondary sources - reviews, treatise, monographs, patents. Web as a source: searching the web. Critical literature review - Identifying gap areas from literature review - Development of working hypothesis. (15 Hours)

Module II

Research design and methods: Research design - Basic Principles - Need for research design — Features of a good design. Important concepts relating to research design: Observation and Facts, Laws and Theories, Prediction and explanation, Induction, Deduction. Development of Models and research plans: Exploration, Description, Diagnosis, Experimentation and sample designs. Data Collection and analysis: Execution of the research - Observation and Collection of data - Methods of data collection - Sampling Methods - Data Processing and Analysis strategies - Data Analysis with Statistical Packages - Hypothesis-Testing - Generalization and Interpretation. (15 Hours)

Module III

Reporting and thesis writing - Structure and components of scientific reports - Types of report - Technical reports and thesis - Significance - Different steps in the preparation, Layout, structure and Language of typical reports, Illustrations and tables, Bibliography, referencing and footnotes. Presentation: Oral presentation - Planning - Preparation - Practice - Making presentation - Use of audio-visual aids - Importance of effective communication. Application of results of research outcome: Environmental impacts - Professional ethics - Ethical issues - Ethical committees. Commercialization of the work - Copyright - royalty - Intellectual
property rights and patent law - Trade Related aspects of Intellectual Property Rights - Reproduction of published material - Plagiarism - Citation and acknowledgement - Reproducibility and accountability. (15 Hours)

References:
1. C.R Kothari, Research Methodology, Sultan Chand & Sons, New Delhi, 1990

Structure of the question paper:

There will be three questions from each module out of which two questions are to be answered by the students.
Structure of the Course

Lecture: 2 hrs/ Week  
Credits: 1
Internal Continuous Assessment: 100 Marks

Course Objectives

- Understand about embedded DSP
- Familiarize DSP processors and FPGA programming for embedded applications

Learning Outcomes

- Ability to program DSP processors
- Ability to implement DSP based solutions for embedded applications

I  
DIGITAL SIGNAL PROCESSING

DSP Programming

1. Familiarization of DSK
2. FFT and Spectrum Estimation
3. Digital Filters
4. PAM and QAM
5. Image Filtering
6. Image Segmentation
7. Denoising and edge detection using DWT

II  
RTOS experiments:

Programs for

1. File Management
2. Process Management
3. Pipes and FIFO
4. Semaphores and Mail Boxes
5. Message Queues and ISRs.
6. Familiarization of SYS/BIOS

III  
FPGA

1. Familiarization of Xilinx/ Altera FPGA
2. Familiarization of simulation, synthesis, Place & Route, Programming
3. Implementation of an ALU
4. Sign Magnitude Adder
5. Floating point Adders
6. Implementation of FIR filter
7. Sine wave generation using LUT/CORDIC approach
8. PWM Generation
9. Design of Traffic light controller
10. LED Time Multiplexing Circuit
11. Stepper Motor and its driver
12. Relay Interface
Structure of the Course
Thesis : 2 hrs/week
Internal Continuous Assessment : 100 Marks

Credits : 2

For the Thesis-Preliminary part-I the student is expected to start the preliminary background studies towards the Thesis by conducting a literature survey in the relevant field. He/she should broadly identify the area of the Thesis work, familiarize with the design and analysis tools required for the Thesis work and plan the experimental platform, if any, required for Thesis work. The student will submit a detailed report of these activities at the end of the semester.

Distribution of marks

Internal assessment of work by the Guide : 50 marks
Internal evaluation by the Committee : 50 Marks
Structure of the Course

Duration : 2 hrs. / Week
Internal Continuous Assessment : 100 Marks

Credits:2

The student is expected to present a seminar in one of the current topics in Electronics, Communication, Instrumentation, Computers, Information Technology, Control systems and related areas with application of Signal Processing. The student will undertake a detailed study based on current published papers, journals, books on the chosen subject and submit seminar report at the end of the semester.

Marks:
- Seminar Report Evaluation : 50 Marks
- Seminar Presentation : 50 Marks
Structure of the Course

Lecture: 3 hrs/ Week
Internal Continuous Assessment: 40 Marks
End Semester Examination: 60 Marks

Course Objectives

• Understand about embedded DSP
• Familiarize DSP processors for embedded applications

Learning Outcomes

• Ability to program DSP processors
• Ability to implement DSP based solutions for embedded applications

Module I: DSP fundamentals programmable fixed point DSPs
Introduction to signal processing systems-Discrete time signals and systems-Linear time invariant systems-DFT-FFT-FIR and IIR filters-Data formats-fixed and floating point DSP-Introduction to programmable DSPs-Bus architecture-Harward and SHARC architectures-Memory access schemes for DSPs-DSP computational building blocks-Special addressing modes-parallel move support and pipe lining

Module II: Programmable fixed point DSPs
Fixed point DSPs from TI-overview of TMS320C54xx-Architecture of ‘C54xx, CPU, MAC unit, Special function units-Interrupts of C54x processor, Internal memory organization, On chip peripherals-Addressing modes and instruction set-Application programs in C for C54x

Module III: Programmable floating point DSPs
Overview of floating point DSPs from TI-Features of TMSC320C6X processors- VelociTI advanced VLIW architecture –TMS320C6713 Floating point processor-features of C6713-Architecture-linear and circular addressing modes-programming in assembly and C-implementation of Digital filters-FFT-digital modulation schemes-image processing.

References:


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
Structure of the Course

Lecture : 3 hrs/ Week
Internal Continuous Assessment : 40 Marks
End Semester Examination : 60 Marks

Course Objectives

- The course is designed to introduce the fundamental concepts of ASIC Design
- Gives an understanding of the different types of Programmable ASICs.
- To give an introduction to architecture and configuration of different FPGA devices
- To understand the goals and objectives of ASIC physical design such as floor planning, placement and routing
- To study the various physical design algorithms for performance optimization
- Gives a brief introduction to SOC Design process, and various techniques to design MPSOCs

Learning Outcomes

- Students will have an understanding of the ASIC Design flow and the various types of ASICs and their implementations.
- Be able to understand the physical design algorithms having a set of objectives and design constraints.
- To understand the SOC design process.

Module I: Introduction to ASIC s, programmable ASICs- programmable ASIC logic I/O cells

Types of ASICs – ASIC Design Flow – Programmable ASICs- Antifuse-SRAM-EPROM-EEPROM based ASICs- practical issues in the use of FPGAs- specifications-Programmable ASIC logic cells and I/O cells - Re-Programmable Devices Architecture- Function blocks, I/O blocks, Interconnects - Architecture and configuration of Spartan III, Spartan 6 and Virtex 5 FPGAs

Module II: ASIC construction, floor planning, placement and Routing

ASIC Design flow- AISC physical design issues- ASIC system partitioning and partitioning methods- ASIC interconnect delay model- Measurement of delay-Floor planning-Placement objectives and algorithms- Routing- Global routing-Detailed routing algorithms- Special routing-Circuit extraction-DRC
Module III: System on-chip design process
SOC Design flow- Waterfall Vs Spiral- Top-Down Vs Bottom Up-specification requirements-system design process—system level design issues-Soft IP Vs Hard IP- MPSoCs. Techniques for designing MPSoCs- Embedded software development for SOC testing-Introduction to Configurable SOC- Hardware/software Co-design methodologies

References:

5. www.xilinx.com
6. www.altera.com

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information

Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
Structure of the Course

Lecture : 3 hrs/ Week
Internal Continuous Assessment : 40 Marks
End Semester Examination : 60 Marks

Course Objectives

• To introduce the students to Linux Embedded OS. The course focuses on the OS structure.
• To introduce about library functions and their underlying mechanisms are introduced.

Learning Outcomes

• The course deals with many facets of the Linux operating system, including:
  Linux kernel structure, I/O, Signals, Processes, Threads, and IPC

Module I: Fundamentals of operating systems

Module II: Introduction to embedded Linux

Module III: Embedded drivers and application porting
References:

3. Mark Mitchell, Jeffrey Oldham and Alex Samuel “Advanced Linux Programming” New Riders Publications

Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TES 2004  EMBEDDED NETWORKING

Structure of the Course

<table>
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</table>

Course Objectives

- Learning of different embedded networking protocols.
- Familiarize various bus standards and embedded networks.

Learning Outcomes

- Able to identify and implement suitable embedded protocols and buses in Embedded System Design.

Module I: Embedded communication protocols


Module II: USB and CAN bus


Module III: Embedded Ethernet


References

2. Jan Axelson, “Parallel Port Complete” , Penram publications
4. Jan Axelson “Embedded Ethernet and Internet Complete”, Penram publications

Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TES 2005 VLSI DIGITAL SIGNAL PROCESSING

Structure of the Course

Lecture : 3 hrs/ Week
Internal Continuous Assessment : 40 Marks
End Semester Examination : 60 Marks

Credits: 3

Course Objectives

- It integrates VLSI architecture theory and algorithms, addresses various architectures at the implementation level.
- It presents several approaches to analysis, estimation, and reduction of power consumption.
- Will help to design high-speed, low-area, and low-power VLSI systems for a broad range of DSP applications.

Learning Outcomes

- Students will be able to apply several optimization techniques to improve implementations of several DSP algorithms, using digital signal processors.
- Students will be able to design and implement in dedicated hardware the various DSP algorithms.

Module I: Introduction to DSP systems
Methods of Representing DSP Systems : Block Diagram -Signal Flow Graph -Dataflow Graph-
Data Dependency Graph -Self-timed Firing-Single-rate and Multi-rate SDFGs -Homogeneous
SDFG –Cyclo-static DFG - Multi-dimensional Arrayed Dataflow Graphs- Control Flow Graphs -
Finite State Machine -Transformations on a Dataflow Graph -Dataflow Interchange Format (DIF) Language -Performance Measures -Iteration Period –loop bound and Iteration bound-

Module II: Architectural transformations
Module III: Algorithm transformations
Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm; Wingrad algorithm-
Iterated convolution-cyclic convolution-Algorithmic strength reduction in filters and transforms-
parallel FIR filters-DCT and IDCT-Pipelined and parallel recursive and adaptive filters -parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters-scaling and round off noise-Synchronous, wave, and asynchronous pipelines

References


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TES 2006 ADVANCED DSP WITH FPGA

Structure of the Course

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<td>End Semester Examination</td>
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</table>

Credits: 3

Course Objectives

- To explain how processor, memory, peripheral components and buses interact in an embedded system.
- To sketch a design of an embedded system around a microprocessor or DSP.

Learning Outcomes

- Able to evaluate how architectural and implementation decisions influence performance and power dissipation.

Module I

Module II
CORDIC Algorithm- Computation of special functions using CORDIC- Vector and rotation mode of CORDIC- CORDIC architectures. Block diagram of a software radio- Digital down converters and demodulators Universal modulator and demodulator using CORDIC- Incoherent demodulation - digital approach for I and Q generation- special sampling schemes- CIC filters

Module III
Residue number system and high speed filters using RNS- Down conversion using discrete Hilbert transform- Undersampling receivers- Coherent demodulation schemes. Speech coding-speech apparatus-Models of vocal tract- Speech coding using linear prediction- CELP coder. An overview of waveform coding- Vocoders- Vocoder attributes- Block diagrams of encoders and decoders of G723.1, G726, G727, G728 and G729

References:


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
Structure of the Course

Lecture : 3 hrs/ Week
Internal Continuous Assessment : 40 Marks
End Semester Examination : 60 Marks

Course Objectives

• Students are introduced communication standards and RTOS.
• Software management and multi-board communication software design is introduced.

Learning Outcomes

• Able to design communication software for embedded systems.

Module I: OSI reference model

Module II: Tables & other data structures

Module III: Multi board communication software design

References
Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
Structure of the Course

Lecture: 3 hrs/Week
Internal Continuous Assessment: 40 Marks
End Semester Examination: 60 Marks

Course Objectives

- Outline validation and testing methodologies for embedded system product
- Formulate an embedded computer system design problem including multiple constraints, create a design that satisfies the constraints

Learning Outcomes

- Able to implement the design in hardware and software.
- Able to measure performance against the design constraints.

Module I
Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Physical defects and their modeling; stuck at faults; Bridging Faults; Fault collapsing. Fault Simulation: Deductive, Parallel and Concurrent; Critical Path Tracing. Test Generation for Combinational Circuits: D-Algorithm, Boolean Difference, PODEM, and ATPG

Module II

Module III

References

5. “VLSI Test Principles and Architectures: Design for Testability” By: Laung-Terng Wang; Cheng-Wen Wu; Xiaoqing Wen
6. “Advanced Simulation and Test Methodologies for Vlsi Design” by Gordon Russell

Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
Structure of the Course

Lecture: 3 hrs/ Week  
Internal Continuous Assessment: 40 Marks  
End Semester Examination: 60 Marks

Course Objectives

- It gives students knowledge of fundamental and state-of-the-art concepts in software-defined radio.  
- Provides the concepts of software radio architectures, existing software radio efforts, a review of basic receiver design principles and application to software radios.  
- Ability to apply SDR in real time applications.

Learning Outcomes

- An ability to make system-level decisions for software-defined radio technology and products.  
- Knowledge of software development methods for embedded wireless systems.

Module I: Concepts and technologies

Module II: Object modeling and software radio
Object modeling-component based approach in software radio- Object oriented representation of radios and network resources- Networks and software radio-object oriented software and software radio-mobile application environments and software radio—SPEAKeasy-JTRS-WITS-UML profile for software defined radio.

Module III: Reconfigurable hardware
Analog to digital conversion for software radio- A/D and D/A architectures-parallel, segmented, iterative and sigma delta structures-smart antennas-structures for beamforming systems-reconfigurable MIMO systems-Digital Hardware Choices-tradeoff using DSP processors-FPGAs and ASICs-reconfigurable Rake receiver-Viginia Tech Adaptive Space Time Radio

References


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
Structure of the Course

Lecture : 3 hrs/ Week
Internal Continuous Assessment : 40 Marks
End Semester Examination : 60 Marks

Credits: 3

Course Objectives

- Learn the basics of designing intelligent agents that can solve general purpose problems.

Learning Outcomes

- Will be able to learn about human machine interface.

Module I


Module II

Embedded agent design criteria & issues - consideration of various solutions- behaviour based methods- behaviour based agent (BBA) mechanisms for implementing reactive functionality in embedded agents - knowledge representation in embedded - BBA mechanisms for implementing deliberative functionality in embedded agents-Multi Embedded Agents - embedded agent coordination mechanisms and benchmarks embedded agent

Module III

Human Machine Issues- HMI interfacing issues in intelligent inhabited environments and their relationships to cognitive disappearance - individuality commercial service issues - technical design consequences arising from social issues such as privacy and Asimov like rules. High end Applications- Case studies- self directed deep space probe - robotic soccer teams - underwater submarines - acrobatic helicopters and mobile robots

References:

2. “Elements of Statistical Learning”- Trevor Hastie, Robert Tibshirani, and Jerome Friedman

Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TED 2001  CRYPTOGRAPHY AND NETWORK SECURITY

Structure of the Course

Lecture : 3 hrs/ Week
Internal Continuous Assessment : 40 Marks
End Semester Examination : 60 Marks

Credits: 3

Course Objectives

- Explain the objectives of information security.
- Analyze the tradeoffs inherent in security.
- Explain the importance and application of each of confidentiality, integrity, and availability.
- Understand the basic categories of threats to computers and networks.
- Discuss issues for creating security policy for a large organization.
- Defend the need for protection and security, and the role of ethical considerations in computer use.

Learning Outcomes

- Design a security solution for a given application.
- Analyze a given system with respect to security of the system.

Module I: Symmetric ciphers

Module II: Network security practice

Module III System security
References


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40 % Theory.
TED 2002 ADVANCED SIGNAL PROCESSING METHODS

Structure of the Course

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<td>End Semester Examination</td>
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Course Objectives

• To have a basic knowledge of concepts, terminology, theories, models and methods for signal processing and the real time applications.
• To gain in-depth knowledge of selected methods in signal processing.

Learning Outcomes

• will gain knowledge about the possibilities and limitations of signal processing systems.
• will be able to implement, analyze and evaluate simple system for signal processing based on the novel algorithms used in signal processing.

Module I

Module II
Redundant Number Representations- Carry-Free Radix-2 Addition and Subtraction- Hybrid Radix-4 Addition- Radix-2 Hybrid Redundant Multiplication - Data Format Conversion- Redundant to Non-Redundant Converter-Numerical Strength Reduction-Sub-Expression Elimination- Multiple Constant Multiplication- Sub-Expression Sharing in Digital Filters- Additive and Multiplicative Number Splitting-Parallel Multipliers-Interleaved Floor-plan and Bit-plan based Digital Filters-Bit-Serial Multipliers-Bit Serial Filter Design and Implementation- Canonic Signed Digit Arithmetic

Module III
References


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
Structure of the Course

Lecture : 3 hrs/ Week 
Internal Continuous Assessment : 40 Marks 
End Semester Examination : 60 Marks 

Course Objectives

- To have a basic knowledge of concepts, terminology, theories, models and methods for digital image processing and the real time applications.
- To gain in-depth knowledge of selected methods in image processing and their DSP implementation.
- To gain practical experience from automatic image processing system.

Learning Outcomes

- will gain knowledge about the possibilities and limitations of built-in image processing systems and therefore be able to estimate which problems can be solved in e.g. industrial and medical applications that can be solved through this technique.
- will be able to implement, analyze and evaluate simple system for automatic image processing, image analysis and computer vision.

Module I: Image processing fundamentals

Module II: Digital signal processors
Overview of floating point DSPs from TI-Features of TMSC320C6X processors- VelociTI advanced VLIW architecture –TMS320C6713 Floating point processor-features of C6713-Architecture-Instruction set- Addressing Modes-linear and circular addressing modes-programming in assembly and C.

Module III: Image processing with DSPS
DSP chips and image processing-tools for image processing with DSP chips-contrast stretching-histogram equalization and specification-linear filtering, median filtering-adaptive filtering-edge detection and segmentation-multiscale edge detection and wavelet denoising of images on DSP chips

References

4. V Udayasankara, ”Real time digital Signal Processing: fundamentals, algorithms, and implementation using TMS processor”, PHI, 2010
5. ShehrzadQureshi, ”Embedded Image Processing on the TMS320C6000 DSP”, Springer, 2005

Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40 % Theory.
TED 2004 ROBOTICS AND MACHINE VISION

Structure of the Course

Lecture : 3 hrs/ Week
Internal Continuous Assessment : 40 Marks
End Semester Examination : 60 Marks

Credits: 3

Course Objectives

- Learn machine vision system design and applications
- Understand camera geometry and calibration
- Learn feature detection and tracking
- Extract 3-D information from single, two, and multiple views
- Estimate camera and object motion

Learning Outcomes

- Will give an exhaustive review of image processing techniques.
- Understand methods commonly found in 3-D vision such as dealing with image noise, feature extraction, 3-D object representation and image matching.

Module I


Module II


Module III

References:


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40 % Theory.
TED 2005  ELECTRONIC PRODUCT DESIGN

Structure of the Course

<table>
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<td><strong>Total Credits</strong></td>
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Course Objectives

- Provide students with a methodical approach to product design which breaks the process down into sequential steps.
- Emphasize the concept that design cannot be carried out in isolation from the manufacturing process, where quality and reliability are essential to economic success.

Learning Outcomes

- Understand the design process, its strengths and weaknesses.
- Have a good working knowledge of a transferable design methodology
- Be able to use response surfaces to optimize processes.
- Understand the impact of process variability on product quality.
- Understand methods for improving quality within an organization.

Module I

Development processes, Identifying customer needs, Establishing product specifications, Concept generation, Concept selection, Product architecture, Industrial design.

Module II


Module III


References

Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TES 3001  
MIXED SIGNAL MODELING

Structure of the Course

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<th>Component</th>
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<td>End Semester Examination</td>
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Credits: 3

Course Objectives

• Understand the mixed signal design methodology.

Learning Outcomes

• Able to incorporate the concepts of mixed signal design in embedded system design.

Module I

Introduction to system design: Dynamic Range, Calibration, Bandwidth, Processor Throughput, Avoiding Excess Speed, Other System Considerations, Sample Rate and Aliasing

DAC & ADC Introduction - converters - High speed ADC design, High speed DAC design and Mixed signal design for radar application - ADC and DAC modules used for LIGO

Module II


Module III

LCD and infra red: LCD Fundamentals, Response Time, Temperature Effects, Connection Methods, Different types of LCD Panels, Static Waveforms, Infra Red Detection and Transmission. TIME-BASED MEASUREMENTS: Measuring Period versus Frequency, Mixing, Voltage-to-Frequency Converters, Clock Resolution and Range, Extending Accuracy with Limited Resolution

References


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TES 3002 LOW POWER VLSI DESIGN

Structure of the Course

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<td>End Semester</td>
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Course Objectives

- To study the concepts on different levels of power estimation and optimization techniques.

Learning Outcomes

- To design chips used for battery-powered systems and high-performance circuits not exceeding power limits.

Module I


Module II

Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library. Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Module III

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package codesign of clock network Algorithm & architectural level methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

References


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TES 3003  CLOUD COMPUTING

Structure of the Course

Lecture: 3 hrs/ Week  Credits: 3
Internal Continuous Assessment: 40 Marks
End Semester Examination: 60 Marks

Course Objectives

• Gives an introduction to cloud computing and its techniques, issues, ecosystem and case studies.
• They can familiar with cloud services and their techniques through labs.

Learning Outcomes

• Large data processing in the cloud.
• Resource management in the cloud and Power management in data centers.
• Monitoring and SLA assurance.

Module I

Module II

Module III
References

2. Barrie Soinsky, "Cloud Computing Bible", Wiley India
3. Kumar Sourabh, "Cloud Computing", Wiley India

Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TES 3004  EMBEDDED SYSTEM DESIGN WITH ARM

Structure of the Course

- Lecture: 3 hrs/ Week
- Internal Continuous Assessment: 40 Marks
- End Semester Examination: 60 Marks

Credits: 3

Course Objectives

- To understand the ARM architecture development,
- To be familiar with embedded system development process.

Learning Outcomes

- Students will be equipped with practical techniques for application development on real ARM hardware.

Module I

Module II

Module III

References

1. Andrew N. Sloss, Dominic Symes, Chris Wright, “ARM System Developer’s Guide”, Morgan
Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
**TES 3005 SOFT COMPUTING TECHNIQUES**

**Structure of the Course**

<table>
<thead>
<tr>
<th>Component</th>
<th>Details</th>
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<tbody>
<tr>
<td>Lecture</td>
<td>3 hrs/ Week</td>
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<tr>
<td>Internal Continuous Assessment</td>
<td>40 Marks</td>
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<tr>
<td>End Semester Examination</td>
<td>60 Marks</td>
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<tr>
<td>Credits</td>
<td>3</td>
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**Course Objectives**

- To introduce the ideas of Neural Networks, fuzzy logic and use of heuristics based on human experience.
- To introduce the concepts of Genetic algorithm and its applications to soft computing using some applications.

**Learning Outcomes**

- To familiarize with soft computing concepts.

**Module I: Introduction**

Approaches to intelligent control- Architecture for intelligent control- Symbolic reasoning system, rule-based systems, the AI approach- Knowledge representation- Expert systems- artificial neural networks- Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron. Learning and Training the neural network- Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations- Hopfield network, Self-organizing network and Recurrent network- Neural Network based controller

**Module II: Fuzzy logic System**

Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning- Introduction to fuzzy logic modeling and control- Fuzzification, inferencing and defuzzification- Fuzzy knowledge and rule bases- Fuzzy modeling and control schemes for nonlinear systems. Self-organizing fuzzy logic control- Fuzzy logic controller for nonlinear time-delay system- Implementation of fuzzy logic controller using Matlab fuzzy-logic toolbox- Stability analysis of fuzzy control systems

**Module III: Genetic Algorithm**

Basic concept of Genetic algorithm and detail algorithmic steps, adjustment of free parameters- Solution of typical control problems using genetic algorithm- Concept on some other search techniques like tabu search and an D-colony search techniques for solving optimization problems- APPLICATIONS GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using Matlab-Neural Network toolbox- Stability analysis of Neural-Network interconnection systems.
References

5. Driankov, Hellendoorn, "Introduction to Fuzzy Control", Narosa Publishers

Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TES 3006 EMBEDDED CONTROL SYSTEMS

Structure of the Course

<table>
<thead>
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<th>Lecture</th>
<th>3 hrs/ Week</th>
<th>Credits: 3</th>
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<tbody>
<tr>
<td>Internal Continuous Assessment</td>
<td>40 Marks</td>
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<tr>
<td>End Semester Examination</td>
<td>60 Marks</td>
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</table>

Course Objectives

- To create computer software and hardware implementations that operate according to well-known standards.

Learning Outcomes

- Able to develop software programs to control embedded system.

Module I

Module II
D/A and A/D conversion: R 2R ladder - Resistor network analysis - Port offsets - Triangle waves analog vs. digital values- ADC0809 – Auto port detect - Recording and playing back voice - Capturing analog information in the timer interrupt service routine - Automatic, multiple channel analog to digital data acquisition

Module III

References:


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
Structure of the Course

Lecture: 3 hrs/ Week
Internal Continuous Assessment: 40 Marks
End Semester Examination: 60 Marks

Credits: 3

Course Objectives

- Understand new theoretical or practical developments and techniques in VLSI design and CAD algorithms.

Learning Outcomes

- Familiarity with computer assisted VLSI design process.

Module I
VLSI physical design automation and Fabrication VLSI Design cycle- New trends in VLSI design-Physical design cycle- Design style- Introduction to fabrication process, design rules-layout of basic devicesVLSI automation Algorithms Partitioning: Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing-Floor planning:Problem formulation, classification of floor planning algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design, chip planning

Module II

Module III
Detailed routing problem formulation, classification of routing algorithms, introduction to single layer routing algorithms, two layer channel routing algorithms, greedy channel routing, switchbox routing algorithms. Over the cell routing & via minimization: Two layers over the cell routers, constrained & unconstrained via minimization-Compaction: Problem formulation, classification of compaction algorithms, one dimensional compaction, two dimension based compaction, hierarchical compaction.

References


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TES  3008  HARDWARE SOFTWARE CO- DESIGN

Structure of the Course

<table>
<thead>
<tr>
<th>Section</th>
<th>Time</th>
<th>Marks</th>
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<tbody>
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<td>Lecture</td>
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</table>

Credits : 3

Course Objectives

- to do hardware/software co-design for embedded systems.
- to develop skills in analysis, approach, optimization, and implementation of embedded systems.

Learning Outcomes

- will be able to analysis, design and testing of systems that include both hardware and software.
- will be able to estimate if additional hardware can accelerate a system.

Module I
Co-design issues: co-design models, architectures, languages, a generic co-design methodology. co-synthesis algorithms: hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis. Prototyping and emulation: prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Module II
Target architectures: architecture specialization techniques, system communication infrastructure, target architecture and application system classes, architecture for control dominated systems (8051-architectures for high performance control), architecture for data dominated systems (adsp21060, tms320c60), mixed systems. Compilation techniques and tools for embedded processor architectures: modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

Module III
Design specification and verification: design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification- languages for system level specification and design: system level specification, design representation for system level synthesis, system level specification languages, heterogeneous specifications and multi language co-simulation.
References:


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TES 3009  FAULT TOLERANT COMPUTING

Structure of the Course

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Course Objectives

- To gain fundamental knowledge and understanding of principles.
- To practice in fault-tolerant computer architecture and computing, emphasizing both hardware and software challenges and the interactions between them.

Learning Outcomes

- Will get exposure to research challenges in this field.

Module I

Fundamental concepts in the theory of reliable computer systems design-Definitions of fault tolerance, fault classification, fault tolerant attributes and system structure-Introduction to redundancy theory, Information redundancy, hardware redundancy, and time redundancy-Limit theorems; decision theory in redundant systems- Dependability Evaluation Techniques: Reliability and availability models: (Combinatorial techniques, Fault-Tree models, Markov models), Performability Models.

Module II

Hardware fault tolerance, redundancy techniques, detection of faults, replication and compression techniques, self-repairing techniques, concentrated and distributed voters, models of fault tolerant computing systems, Case studies. Software fault tolerance: fault tolerance versus fault intolerance, errors and their management strategies. Implementation techniques: software defense, protective redundancy, architectural support.

Module III


REFERENCE

Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
TES 3010 ADHOC NETWORKS

Structure of the Course

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Course Objectives

- To introduce and study established and emerging areas of wireless networking.
- The focus will be on network protocols above the physical layer, such as the media access control and the network layer.

Learning Outcomes

- To concentrate on the synchronization aspects of cooperative transmission
- To address quality of service issues and network reliability for transmission of real-time information.

Module I


Module II


Module III

Energy Management: Need, classification of battery management schemes, Transmission power management schemes, System power management schemes- Wireless Sensor Networks: Architecture, Data dissemination, Date gathering, MAC protocols, location discovery, Quality of a sensor network- Performance Analysis  ABR beaconing, Performance parameters, Route-
discovery time, End-to-end delay performance, Communication throughput performance, Packet loss performance, Route reconfiguration/repair time, TCP/IP based applications

References


Structure of Question Paper

There will be three questions carrying 10 marks each from each module out of which two questions are to be answered by the students. The question paper will consist of 60% problems and 40% Theory.
THESIS PRELIMINARY PART II

Structure of the Course

Thesis : 14 hrs/week  
Credits: 5
Internal Continuous Assessment : 200 Marks

The Thesis Preliminary Part - II is an extension of Thesis Preliminary Part - I. Thesis Preliminary Part II comprises preliminary thesis work, two seminars and submission of Thesis - Preliminary report. The first seminar would highlight the topic, objectives and methodology and the second seminar will be a presentation of the work they have completed till the third semester and the scope of the work which is to be accomplished in the fourth semester, mentioning the expected results.

Distribution of marks

Internal assessment of work by the Guide : 100 Marks
Internal evaluation by the Committee : 100 marks
TEC 4101

THESIS

Structure of the Course

Thesis : 21 hrs/week
Internal Continuous Assessment : 300 Marks
End Semester Examination : 300 Marks

Credits: 12

The student has to continue the thesis work done in second and third semesters. There would be an interim presentation at the first half of the semester to evaluate the progress of the work and at the end of the semester there would be a pre-Submission seminar before the Evaluation committee for assessing the quality and quantum of work. This would be the qualifying exercise for the students for getting approval from the Department Committee for the submission of Thesis. At least once technical paper is to be prepared for possible publication in Journals/Conferences. The final evaluation of the Thesis would be conducted by the board of examiners constituted by the University including the guide and the external examiner.

Distribution of marks

Internal evaluation of the Thesis work by the Guide : 150 Marks
Internal evaluation of the Thesis by the Evaluation Committee : 150 Marks
Final evaluation of the Thesis Work by the Internal and External Examiners:
[Evaluation of Thesis: 200 marks *+ Viva Voce: 100 marks (*5% of the marks is earmarked for publication in Journal/Conference)] TOTAL – 300 Marks