Fourth Semester B.Tech Degree Examination, April 2015

(2013 scheme)

13.403 COMPUTER ORGANISATION & ARCHITECTURE (AT)

(Model Question Paper)

Time:3 Hours Max.Marks:100

PART-A (10 x2 =20)

(Answer all questions)

1. Explain R-type instruction format using an example
2. State the addressing mode used for the instruction
   beq $s1,$s2,25
3. Explain the advantages of edge triggered clocking methodology
4. State the difference of the instructions :
   j 2500
   jal 2500
5. Show the data path for instruction fetch.
6. How are blocks in cache replaced?
7. What is memory interleaving?
8. Briefly explain RAID.
9. What do you mean by stall?
10. What are priority interrupts?

PART-B

(Explain anyone full question from each module)

Module I

11. a).Explain the hardware implementation of restoring division algorithm , Also divide 1001 by 0010 using restoring division algorithm (10)

    b). Multiply the following numbers with necessary steps (10)

    (i) 0.4_{10} and -0.5332_{10}

    (ii) $9.99_{10} \times 10^{10}$ and $1.61_{10} \times 10^{-2}$

12. a). Explain the following (10)

(i) Harvard and Von-Neumann architecture with examples

(ii) How to load 32 bit constant value to a register

b). Convert the following C program into MIPS assembly code (10)

```
Swap (int v[], int k);
{  int  temp;
   temp =v[k];
    v[k] =v[k+1];
    v[k+1]=temp;
    }
```

Module II

13 . a). Explain the complete data path for the multicycle implementation with the help of block diagram showing the necessary control lines. (10)

b). Which are the steps involved in the execution of MIPS instructions? Give examples (10)

14. a). Differentiate between single cycle and multicycle implementation. State the disadvantages of single cycle Implementation (10)

b). Compare the features of micro programmed and hardwired control unit (10)

Module III

15 a). Write short notes on cache miss, cache hit, miss penalty, hit rate . Explain methods to reduce cache miss (10)

b). Explain how address translation is carried out in virtual memories. List the advantages and disadvantages of using virtual memory. (10)

16. a). Draw the structure of memory hierarchy. Explain SRAM and DRAM with neat diagram. (10)

b). Explain different types of ROM .Implement (64 x 8) ROM using (16 x 8) ROM modules (10)

Module IV

17. a). How is data transferred directly between memory and I/O device without the involvement of processor? How is it different from other I/O device? (10)

    b). What is handshaking ? Explain asynchronous hand shaking protocol with signal diagrams (10)

18. a). Explain pipelined data path with neat diagram. How does it improve the performance of the system? (10)

    b). Explain hazards in pipeline architecture .How they are overcome? (10)